REMARKS

Claims 1 – 34 are pending, and claims 1 – 34 stand rejected. Claims 8, 9, 25, and 26 have been amended. The applicant respectively traverses the rejection and request allowance of claims 1 – 34.

Claims 1 – 5, and 18 - 22 are rejected under 35 U.S.C 102(b) as being anticipated by Yu et. al. (US 6,504,846). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California,* 2 USPQ2d 1051, 1053 (Fed Cir. 1987). Claim 1 requires:

"a pointer cache configured to *store pointers* that correspond to external buffers that are external to the integrated circuit and are configured to store the communication packets; and,

control logic configured to *allocate the external buffers as the corresponding pointers are read from the pointer cache* and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache." (emphasis added)

Yu has a cache, but the cache in Yu does not store pointers. The cache in Yu stores "a value corresponding to the number of copies of the received data frame that must be transmitted" (see column 15, lines 55 – 58). There is a one-to-one correspondence between the number of entries in Yu's cache and the number of frame buffers, but the entries in Yu's cache don't point to each frame buffer. Furthermore, when a data frame is successfully transmitted, the value in the cache is read and decremented. Once the value reaches zero, a frame pointer is transferred into the free buffer queue (see column 17, lines 47 – 53). Because the value in the cache in Yu may be read multiple times (each time a data frame is successfully transmitted) it is apparent that an external

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buffer will not be allocated each time the cache is read. Claim 1 requires that an external buffer is allocated when the pointer in the cache is read.

Because Yu does not contain a cache that is configured to stores pointers, as required by claim 1, the examiner has not established the requirements for a *prima facie* case of anticipation. Therefore Claim 1 is allowable as written.

Claims 2 – 17 depend on allowable claim 1. Therefore claims 2 – 17 are also allowable.

Claim 18 also has a limitation that pointers must be stored in a cache. Therefore the arguments for claim 1 (above) apply to claim 18 and claim 18 is allowable as written.

Claims 19 – 34 depend on allowable claim 18. Therefore claims 19 – 34 are also allowable.

The prior art made of record and not relied upon has been reviewed and is not considered relevant.
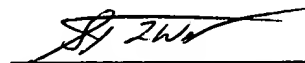
Conclusion

Based on the above remarks, the Applicants submit that claims 1 - 34 are allowable. There may be additional reasons in support of patentability, but such reasons are omitted in the interests of brevity. The Applicants respectfully request allowance of claims 1 - 34.

Any fees may be charged to deposit account 502622.

Respectfully submitted,

Date: 1/29/04

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